SEMICONDUCTOR PACKAGE WITH THERMAL ENHANCE FILM AND MANUFACTURING METHOD THEREOF

BACKGROUND OF THE INVENTION

Field of Invention

[0001] This invention relates to a semiconductor package. More particularly, the present invention is related to a semiconductor package with a thermal enhance film and manufacturing method thereof.

Related Art

[0002] Originally, a semiconductor package is formed by the processes of singulating a wafer into a plurality of semiconductor chips, attaching one of the semiconductor chips onto a substrate and electrically connecting the semiconductor chip to the substrate via a plurality of conductive wires, encapsulating the semiconductor chip, the substrate and the conductive wires by an encapsulation. Similarly, the semiconductor package also can be formed by the method of flip chip bonding. However, the wafer is made of a material selected from silicon, which is crumbly. Accordingly, the active surface of the wafer is easily to be broken and chipping so as to cause the electrical circuits to be shortened and damaged.

[0003] Therefore, providing another semiconductor package and a manufacturing method thereof to solve the mentioned-above disadvantages is the most important task in this invention.

SUMMARY OF THE INVENTION

[0004] In view of the above-mentioned problems, an objective of this invention is

to provide a thermal enhance film formed on the back surface of the semiconductor chip and a manufacturing method thereof to upgrade the efficiency of the heat transmission of the semiconductor package.

[0005] Moreover, another object of this invention is to provide a polymer film, formed on a back surface of a wafer prior to the process of singulating the wafer into a plurality of semiconductor chips so as to prevent the active surface of the wafer from being chipping.

[0006] To achieve the above-mentioned objective, a semiconductor package is provided, wherein the semiconductor package mainly comprises a substrate, a semiconductor chip and a thermal enhance film. Therein the semiconductor chip is electrically connected to the substrate via a plurality of bumps and the thermal enhance film is formed on the back surface of the semiconductor chip. The thermal enhance film has metal powder, thermally conductive powder therein or is made of thermally conductive material, for example a thermally conductive tape, a thermally conductive epoxy and a thermally conductive polymer film, so the efficiency of the heat transmission of the semiconductor package can be upgraded.

[0007] As mentioned above and to achieve another above-mentioned objective, the thermal enhance film can be made of polymer. Namely, a thermally conductive polymer film can be formed on the back surface of the wafer prior to the process of singulating the wafer into a plurality of semiconductor chips, so the active surface of the wafer will be prevented from being chipping when the singulation process is performed. Thereby the active surface of the wafer can be prevented from being chipping by the thermally conductive polymer film in that the polymer film is provided as a buffer layer on the back surface of the wafer when the wafer is singulated or cut.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The invention will become more fully understood from the detailed description given herein below illustrations only, and thus are not limitative of the present invention, and wherein:

[0009] FIG. 1 is a cross-sectional view of a semiconductor package with a thermal enhance film according to the first embodiment of the present package;

[0010] FIG. 2 is a cross-sectional view of a semiconductor package with a thermal enhance film according to the second embodiment of the present package;

[0011] FIG. 3 is a cross-sectional view of a semiconductor package with a thermal enhance film according to the third embodiment of the present package;

[0012] FIG. 4 is a cross-sectional view of a semiconductor package with a thermal enhance film according to the fourth embodiment of the present package;

[0013] FIG. 5 is a cross-sectional view of a semiconductor package with a thermal enhance film according to the fifth embodiment of the present package;

[0014] FIG. 6 is a cross-sectional view of a semiconductor package with a thermal enhance film according to the sixth embodiment of the present package; and

[0015] FIG. 7 is a flow chart illustrating the process flow of a manufacturing method of the semiconductor package of FIG. 1.

DETAILED DESCRIPTION OF THE INVENTION

[0016] The semiconductor package with a thermal enhance film and a manufacturing method thereof according to the preferred embodiment of this

invention will be described herein below with reference to the accompanying drawings, wherein the same reference numbers refer to the same elements.

[0017] In accordance with a first preferred embodiment as shown in FIG. 1, there is provided a semiconductor package with a thermal enhance layer. The semiconductor package mainly comprises a substrate 11, a semiconductor chip 12 and a thermal enhance layer 13. The substrate 11 has an upper surface 111 and an opposite lower surface 112. The semiconductor chip 12 has an active surface 121, a back surface 122, a plurality of bonding pads 123 formed thereon, and a plurality of bumps 124, for example solder bumps and gold bumps, formed on the bonding pads 123. Besides, the thermal enhance layer 13, for example a thermal enhance film, a thermal enhance tape, a thermally conductive epoxy, and a thermally conductive polymer layer, is formed on the back surface 122 of the semiconductor chip 12. The coefficient of thermal expansion of the substrate 11 is different from that of the semiconductor chip 12, so an underfill 14 or similar fillers are disposed at a gap between the substrate 11 and the semiconductor chip 12 to prevent the substrate 11 and the semiconductor chip 12 from being damaged by the thermal stress caused by the change of the temperature. In addition, a plurality of solder balls 15 are mounted on the lower surface 112 of the substrate 11 so as to be an electrical connection path to electrical connect to external devices.

[0018] As mentioned above, when the thermal enhance layer 13 is a thermally conductive epoxy, it can be formed on the back surface 122 of the semiconductor chip 12 by the method of screen-printing. Moreover, when the thermal enhance layer 13 is a thermally conductive tape or thermally conductive film, it can be directly attached on the back surface 122 of the semiconductor chip 12.

[0019] Next, referring to FIG. 2., a second preferred embodiment is shown. When

the thermal enhance layer 13 is made of thermally conductive epoxy and before the thermally conductive epoxy is fully cured, the thermally conductive epoxy is also regarded as an adhesive. Thus a heat spreader 16 with a cap-like shape can be connected to the back surface 122 of the semiconductor chip 12 via the thermally conductive epoxy and attached to the upper surface 111 of the substrate 11 via another adhesive17. Therefore, the heat arisen out of the semiconductor chip 12 can be transmitted to the outside via the heat spreader 16 and the thermal enhance layer 13 (thermally conductive epoxy), and the efficiency of the heat transmission of the semiconductor package will be upgraded.

[0020] Similar to the above mentioned, a third embodiment is shown in FIG. 3. In FIG. 3, a heat spreader 18 with a flat shape is attached to the back surface 122 of the semiconductor chip 12 via the thermal enhance layer 13 in order to upgrade the efficiency of the heat transmission of the semiconductor package. Besides, a stiffener ring 19 is disposed on the substrate 11 and surrounds the semiconductor chip 12 so as to be a supporter to support the heat spreader 18 and to prevent the heat spreader 18 from being tilted and deformed.

[0021] Furthermore, a fourth embodiment is shown in FIG. 4, a semiconductor chip 12 with a thermal enhance layer 13 formed on the back surface 122 thereof is disposed on the lower surface 112 of the substrate 11.

[0022] Next, a fifth embodiment is provided in FIG. 5. Two semiconductor chips 12 are disposed on the upper surface 111 of the substrate 11 and another semiconductor chip 12 is disposed on the lower surface 112 of the substrate 11. Therein the semiconductor chips all has a thermal enhance layer 13 formed on the back surface 122 of each semiconductor chip 12. Besides, the semiconductor chip 12 can be electrically connected to the substrate via conductive wires (not shown).

[0023] Moreover, as shown in FIG. 6, a sixth embodiment of this invention is provided. The substrate 11 has an opening 113 and the semiconductor chip 12 with a thermal enhance layer 13 is disposed in the opening 113 and electrically connected to the substrate 11 via conductive wires 125, for example gold wires. Finally, an encapsulation 20 encapsulates the semiconductor chip 12 and the conductive wires 125, and exposes the thermal enhance layer 13. Thus the heat arisen out of the semiconductor chip 12 can be transmitted to the outside through the thermal enhance layer 13. It is should be noted that the reference numeral of each element in FIG. 2, 3, 4, 5 and 6 corresponds to the same reference numeral of each element in FIG. 1.

[0024] Next, referring to FIG. 7, a flow chart of the manufacturing method of the semiconductor package is disclosed. First, in step 71, a substrate having a plurality of substrate units, for example an organic substrate and a ceramic substrate, is provided. Then, in step 72, a wafer, having a plurality of semiconductor chips, with an active surface and a back surface is provided. Therein a thermal enhance layer is formed on the back surface of the wafer and a plurality of bonding pads formed on the active surface of the wafer. Furthermore, the active surface of the wafer faces the upper surface of the substrate and electrically connects to the substrate via a plurality of bumps. Afterwards, in step 73, an underfill is filled into a gap between the wafer and the substrate so as to prevent the semiconductor package from being damaged by CTE mismatch. Finally, in step 74, the wafer and the substrate are singulated by cutting simultaneously so as to form a plurality of semiconductor packages at least having one of the substrate units and one of the semiconductor chips.

[0025] As mentioned above, the thermal enhance layer is a thermally conductive polymer layer and formed on the back surface of the wafer. Accordingly, in step 73, when the wafer is singulated by cutting, the thermal enhance layer can be regarded as

a buffer layer to prevent the active surface of the wafer from being chipping and damaged.

[0026] Besides, after step 74 is performed, a step of attaching a heat spreader on the back surface of the semiconductor chip can be performed to increase the efficiency of the heat transmission of the semiconductor package.

[0027] Although the invention has been described in considerable detail with reference to certain preferred embodiments, it will be appreciated and understood that various changes and modifications may be made without departing from the spirit and scope of the invention as defined in the appended claims.